СЕНСОРИ ФІЗИЧНИХ ВЕЛИЧИН

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ELECTRICAL PROPERTIES OF FINFET STRUCTURES

T. E. Rudenko[1], V. I. Kilchytska[1, 2], N. Collaert[3], M. Jurczak[3], A. N . Nazarov[1], V. S. Lysenko[1], and D. Flandre[2]

[1]Institute of Semiconductor Physics, NAS of Ukraine, Prospect Nauki 45, 03028 Kyiv, Ukraine
E- mail:tamara@lab15.kiev.ua
[2]Laboratoire de Microйlectronique, Universitй catholique de Louvain,
Place du Levant 3, 1348 Louvain-la-Neuve, Belgium
[3]InterUniversity Microelectronics Center (IMEC), Kapeldreef 75, 3001 Leuven, Belgium

Abstract

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Electrical properties of FinFET (fin field-effect-transistor) structures are investigated. These structures are considered to be the most promising candidates for the creation of nano-scale metal-oxide-semiconductor (MOS) devices and integrated circuits due to strong suppression of the short-channel effects. The impact of the structure dimensions on the characteristics of the transistors is studied. Particular attention is given to the carrier mobility in the inversion channel of FinFET structures.

Key words: Metal-oxide-semiconductor (MOS) transistor; semiconductor on insulator (SOI); nano-scale devices; FinFET (fin field-effect-transistor).

Анотація

ЕЛЕКТРИЧНІ ВЛАСТИВОСТІ FINFET СТРУКТУР

Т. О. Руденко, В. І. Кільчицька, Н. Коллаерт, М. Юрчак, О. М. Назаров, В. С. Лисенко, Д. Фландр

Досліджено електричні властивості транзисторних структур типу FinFET (fin field-effect-transistor). Ці структури вважаються найбільш перспективними для створення нано-розмірних метал-оксид-напівпровідник (МОН) транзисторів і інтегральних схем завдяки значному послабленню коротко-канальних ефектів. Досліджено вплив геометричних розмірів структури на характеристики транзисторів. Особливу увагу приділено рухливості носіїв в інверсійному каналі FinFET структур.

Ключові слова: Метал-оксид-напівпровідник (МОН) транзистор; кремній на ізоляторі (КНІ); нано-розмірні прилади; FinFET (fin field-effect-transistor).

Аннотация

ЭЛЕКТРИЧЕСКИЕ СВОЙСТВА FINFET СТРУКТУР

Т. Е. Руденко, В. И. Кильчицкая, Н. Коллаерт, М. Юрчак, А. Н. Назаров, В. С. Лысенко, Д. Фландр

Исследованы электрические свойства транзисторных структур типа FinFET (fin field-effect-transistor). Эти структуры считаются наиболее перспективными для создания нано-размерных металл–окисел-полупроводник (МОП) транзисторов и интегральных схем благодаря сильному подавлению коротко-канальных эффектов. Исследовано влияние геометрических размеров структуры на характеристики транзисторов. Особое внимание уделено подвижности носителей в инверсионном канале FinFET структур.

Ключевые слова: Металл-окисел-полупроводник (МОП) транзистор; кремний на изоляторе; нано-размерные приборы; FinFET (fin field-effect-transistor).

1. Introduction

Scaling of CMOS into nano-meter region led to the development of new device structures. Suitable candidates are silicon-on-insulator (SOI) devices with multiple gates such as double-gate, triple-gate, Omega-gate, gate-all-around FET structures, which can be scaled more aggressively than conventional planar bulk-Si devices. The key feature of all these multi-gate SOI MOSFETs is strong gate control of the channel region due to the thin Si bodies, effectively suppressing short-channel effects, even without using high channel doping. Amongst different multi-gate structures, the FinFET is considered to be the most promising candidate for future nano-scaled devices because of its excellent scalability, along with relatively simple fabrication [1]-[3]. Therefore electrical characteristics of FinFETs are of great interest.

In this work, the electrical characteristics of the advanced FinFET structures with high-K gate dielectrics and mid-gap gate electrodes are studied, focusing on the FinFET mobility. Due to a three-dimensional device nature and location of the top and lateral channels in different crystallographic planes, the mobility behaviour in FinFETs can be different from that in single-gate and double-gate devices. In a given work, for better understanding of the FinFET mobility, we study the effective mobility in narrow-fin devices versus quasi-planar (very wide-fin) devices, and as a function of the fin width (down to 25 nm).

2. Device description

The devices studied were processed at IMEC. The triple-gate FinFETs with Ω-configuration and metal gate electrodes were fabricated on SOI wafers featuring a 65 nm-thick Si film on 145-nm of buried oxide. Details of fabrication processes are described in [4]. The gate covered three sides of the fin, as shown in Fig. 1, creating a channel on each side: the top channel and the two lateral channels, lying, respectively, in (100) and (110) crystallographic planes.

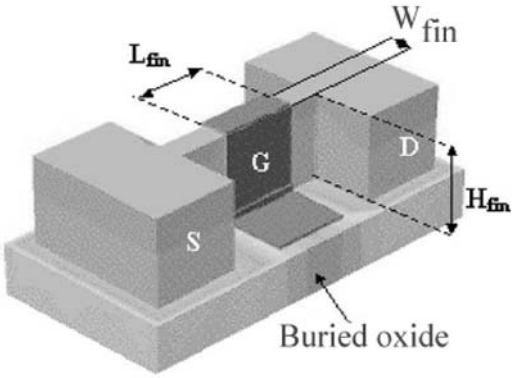

Fig. 1. Schematic representation of the FinFET architecture.

In this study, the devices with different gate stacks were used. In one of them, the gate stack consisted of a plasma nitrided oxide (SiON) with 1.8 nm equivalent oxide thickness of and chemical vapor deposited (CVD) TiN, as a gate electrode. The devices studied were n- and p-channel 5-fin FETs with a fin height H_{fin}=60 nm and fin width W_{fin} varying from 3 μm down to 25 nm. No channel doping was used in these devices. The SEM photographs of the top and cross section of the FinFETs with W_{fin}=25 nm are shown in Fig. 2.

Another set of the devices had an atomic layer deposited (ALD) TaN gate electrode and two types of gate dielectrics, namely, a nitrided oxide (SiON) with 1.8 nm equivalent oxide thickness and

ALD HfO_2 deposited on a chemical oxide with total equivalent oxide thickness of 1.6 nm. The TaN gate devices received a channel implant to provide channel doping ~10^{18} cm^{-3}. The measured devices were multiple-fin FETs consisting of 30 fins with H_{fin}=50 nm and W_{fin}=45 nm. Comparative measurements were performed on very wide single-fin (W_{fin}=10 μm) structures.

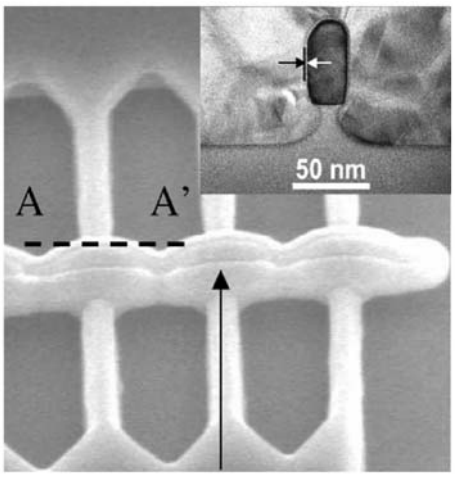

Fig. 2. The SEM photographs of the top and cross section of the FinFETs with W_{fin}=25 nm.

In this study, devices with the gate length L_g from 20 μm down to 40 nm were measured. However, for mobility measurements only very long devices (L_g=10-20 μm) were used to avoid short-channel and series resistance effects. All measurements were performed at room temperature.

3. Impact of the fin width on the short-channel effects

The short-channel effects in a MOSFET are usually characterized by the threshold voltage (V_{th}) roll-off and degradation of subthreshold slope with shrinking the gate length. A key advantage of FinFETs is the reduction of the short-channel effects by decreasing the fin width without use of high channel doping. This is illustrated by Fig. 3 (a), showing the comparison of the subthreshold drain current (I_d) versus gate voltage (V_g) characteristics of the undoped very short n-channel devices (L_g=80 nm) with different fin widths. The inset in Fig.3 (a) shows the inverse subthreshold slope S as a function of the fin width. A clear improvement of the subthreshold characteristics of the short-channel device is observed when W_{fin} is reduced, namely: the subthreshold slope becomes steeper (i.e., S decreases), the off-state current reduces, and V_{th} increases, approaching its long-channel value. Fig. 3(b) shows degradation of the subthreshold characteristics in the narrow-fin devices (W_{fin}=25 nm) with decreasing the gate length from 1 μm to 40 nm. The inset in Fig. 3(b) shows the corresponding degradation of the subthreshold slope. From Fig. 3(b) it is seen that the behavior of the $I_d(V_g)$-characteristics of very narrow-fin devices (with W_{fin}=25 nm) remains the same as in long-channel devices, showing invariable V_{th} and excellent S=61-64 mV/decade, when the gate length reduces down to L_g=60 nm. These measurements fully support theoretical predictions, which show that adequate suppression of the short-channel effects in a FinFET can be reached if the fin width is ≤2/3 of the gate length [2], [3].

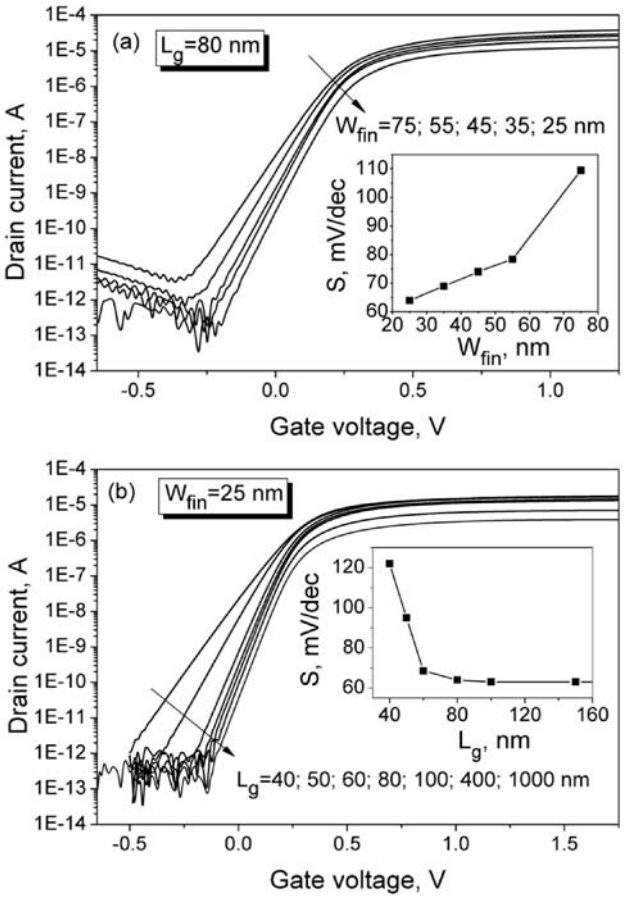

Fig. 3. Subthreshold characteristics of undoped n-channel FinFETs with: (a) L_g=80 nm and different fin widths; (b) W_{fin}=25 nm and different gate lengths. The inset in Fig. 3(a) shows the inverse subthreshold slope as a function of the fin width, and in Fig. 3(b) as a function of the gate length. Measurements are performed on 5-fin devices with the TiN/SiON gate stack.

4. Effective channel mobility

4.1. Factors affecting the FinFET mobility

Amongst the factors which can affect the FinFET mobility, the different crystallographic orientation of the top and lateral channels is most important. The sidewall channels in FinFETs fabricated on a standard (100) wafer lie typically in a (110) plane. In a narrow-fin FET, in which the fin width is less than the fin height ($W_{fin}<H_{fin}$), the conduction is mainly determined by side channels. Thus, due to anisotropy of the effective masses, hole mobility in FinFETs is expected to be enhanced, while electron mobility to be degraded compared to conventional planar devices with the (100) surface orientation. Besides, the effective mobility in FinFETs can be affected by volume inversion at low charge densities, fin roughness, and, in the case of doped channel, different doping levels of the fin top and sides.

4.2. Mobility extraction procedure

The effective mobility, μ_{eff}, in a MOSFET is traditionally defined from the drain current I_d measured at low drain voltage V_d, as follows:

$$\mu_{eff} = \frac{I_d}{(W/L)\cdot V_d \cdot q \cdot N_{inv}}, \qquad (1)$$

where W and L are, respectively, channel width and length, N_{inv} is the inversion carrier density per unit gate area, q is the electron charge. In this work, N_{inv} was experimentally determined using a split C-V technique, which is usually used for MOSFETs with ultra-thin gate dielectrics [5]. In a split C-V technique, N_{inv} is determined from the measured gate-to-channel capacitance C_{gc} and its normalizing to the gate area:

$$N_{inv} = \frac{1}{q}\cdot\int_{V_{acc}}^{V_g}\frac{C_{gc}(V_g)}{W\cdot L}dV_g, \qquad (2)$$

where C_{gc} is the gate-to-channel capacitance *per whole gate area,* V_g is the gate voltage, and V_{acc} is the gate voltage in accumulation, where N_{inv}=0. From Eqs.(1) and (2), μ_{eff} can be obtained as:

$$\mu_{eff}(V_g) = \frac{L^2\cdot I_d}{V_d\cdot\int_{V_{acc}}^{V_g} C_{gc}(V_g)dV_g}. \qquad (3)$$

From Eq. (3) it follows that with the split C-V measurements, $\mu_{eff}(V_g)$ can be determined without knowledge of both the dielectric thickness and channel width, which is particularly important in the case of FinFETs, in which both are not reliably known. However, when plotting μ_{eff} as a function of N_{inv}, it is neccessary to know the device channel width. In this work, the channel width in a FinFET was defined as: W=*number of fins* × $(2H_{fin} + W_{fin})$.

4.3. Mobility in TaN gate FinFETs with doped-channel

Fig. 4 (a), (b) shows the effective hole (μ_p) and electron (μ_n) mobilities as a function of the inversion carrier density obtained in TaN gate narrow-fin devices (W_{fin}=45 nm) and quasi-planar very wide-fin devices (W_{fin}=10 μm) with highly-doped channel and two types of the gate dielectrics. It is evident from Fig. 4(a) that for both SiON and HfO_2 gate dielectrics, μ_p in narrow-fin devices determined mainly by (110)-oriented fin sidewalls is significantly higher (~2.5 times) than that in counterpart quasi-planar (very wide-fin) devices, determined by the (100) top channel mobility, as expected due to anisotropy of the effective masses. For the same reason, one might expect that electron mobility in narrow FinFETs to be degraded compared to that in quasi-planar devices. However, as is seen from Fig. 4 (b), contrary to expectations, at moderate and low N_{inv}, the effective μ_n in narrow FinFETs with highly doped channel is also much higher than in their counterpart quasi-planar devices. This enhancement of μ_n in narrow FinFETs, which reaches factor of 3 at low N_{inv} and vanishes at high N_{inv}, is attributed to lower doping of the fin sidewalls compared to the fin top, resulting in the lower Coulomb scattering and lower transverse electric field E_{eff}, as well as to fully-depleted double-gate-like operation of narrow FinFETs, also reducing E_{eff}. These two factors improve also hole mobility at low N_{inv}. Such behavior observed for both metal gate devices [6] and poly-Si gate devices [7].

4.4. Mobility in undoped-channel FinFETs with TiN gate and various fin widths

Fig. 5 presents μ_p and μ_n as a function of N_{inv} in undoped-channel FETs with various W_{fin}. For undoped channel, the enhancement of μ_p and degradation of μ_n, in narrow FinFETs are observed, as compared to quasi-planar wide-fin devices, which can be attributed to surface orientation effect of the top and lateral channels. The behavior of the FinFET mobility in respect to the fin width is different in different regions of N_{inv}. In the high N_{inv} region, where N_{inv} >6x10^{12} cm^{-2}, the fin width dependence of both μ_p and μ_n with W_{fin} can be attributed to variation

of the relative contributions of top and lateral conduction channels, having different mobilities due to different surface orientation. In this high N_{inv} region, the FinFET mobility is presumably controlled by the surface roughness scattering. However, at lower N_{inv}, the μ_n behavior in a FinFET is more complicated, that is, the conduction of the device cannot be presented simply as a sum of the top and lateral conduction channels. It is assumed that in the N_{inv} range of the maximum μ_n in FinFETs (where μ_n slightly increases with decreasing W_{fin} from 75 nm to 25 nm), μ_n is governed mainly by phonon scattering, while at lower N_{inv}, where μ_n strongly decreases with decreasing N_{inv} and W_{fin}, the dominant scattering mechanism is Coulomb scattering. A stronger degradation of μ_n with decreasing W_{fin} at low N_{inv}, as compared to the predicted and measured degradation in ultra-thin body and double-gate SOI devices for the same body thickness range [8], might be attributed to the fact that in tri-gate FinFETs, carriers can be simultaneously affected by four Si-SiO_2 interfaces.

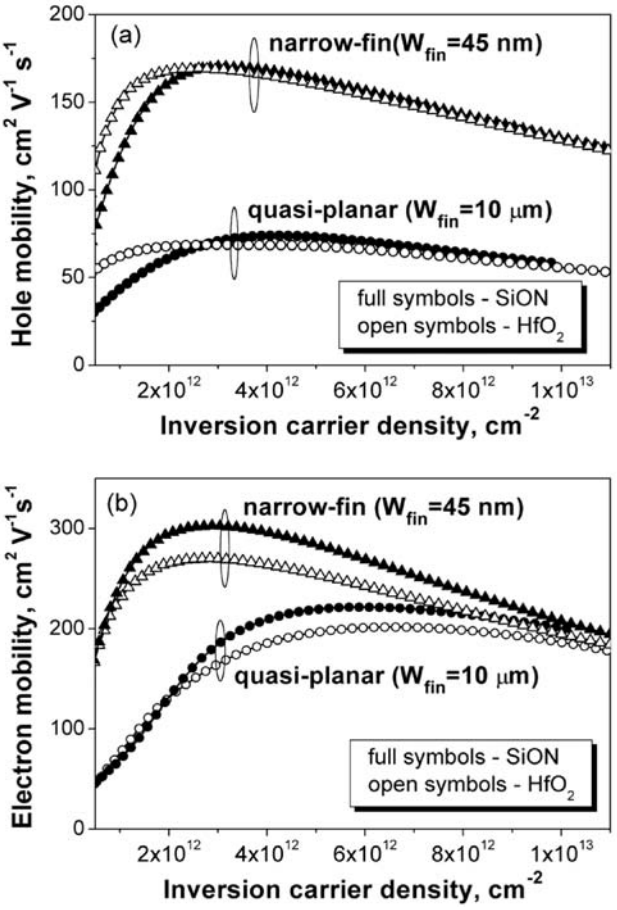

Fig. 4. The effective hole (a) and electron (b) mobility in TaN gate narrow-fin devices (W_{fin}=45 nm) and quasi-planar very wide-fin devices (W_{fin}=10 μm) with highly doped channel plotted as a function of the inversion carrier density.

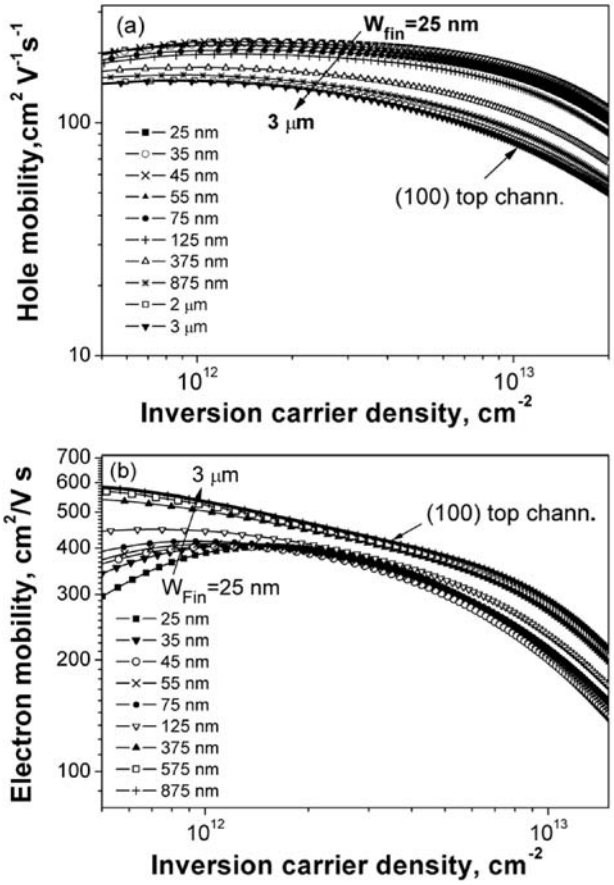

Fig. 5. The effective hole (a) and electron (b) mobilities in undoped-channel devices with various W_{fin} (TiN/SiON, H_{fin}=60 nm, L_g=10 μm).

5. Conclusions

The behavior of the effective mobility in narrow FinFET structures was studied as compared to quasi-planar very wide-fin structures, and as a function of the fin width. It is found that doped-channel narrow FinFET structures reveal a strong enhancement of hole mobility (more than twice) in narrow FinFET devices compared to their counterpart quasi-planar very wide-fin devices, as expected due to a (110) orientation of fin sidewalls, and also surprising enhancement of electron mobility, attributed to lower doping of fin sides and fully-depleted double-gate-like operation of narrow FinFETs, resulting in lower Coulomb scattering and lower effective electric field.

Undoped-channel narrow FinFETs exhibit higher hole mobility and lower electron mobility, as compared to those in quasi-planar (very wide-fin) SOI devices, which has been attributed to different surface orientation of the fin top and sides. At high

inversion carrier densities, impact of the fin width on the effective mobility in a triple-gate FinFET has been explained by the variations of the relative contributions of top and lateral conduction channels. A strong decrease in the electron mobility with reducing the fin width observed at low carrier densities has been explained by Coulomb scattering, enhanced due to interaction with four Si-SiO_2 interfaces.

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