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ELECTRONIC PROPERTIES OF THE FET STRUCTURES WITH QDS LAYER UNDER THE GATE AREA

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Abstract. The field-effect transistor (FET) structures with quantum dots (QDs) layer placed close to the high electron mobility channel on the heterojunction GaAs/AlGaAs are investigated in this paper. It was shown that charge accumulated in QDs layer can essentially change the threshold voltage value needed to open the channel. Because of kinetic nature of capturing and emitting processes in QDs the differential capacitance measured between Source and Gate has the specific view with several maximums on C-V curves depending of the frequency of testing signal. Due to influence of charge accumulation in QDs on the coefficient of transmission for the transistors with QDs layer under the gate the FET structure demonstrates the effect of dynamical changing of channel conductivity.

Keywords: field-effect transistors, quantum dots, GaAs/AlGaAs

ЕЛЕКТРОННІ ВЛАСТИВОСТІ ПТ СТРУКТУР З ШАРОМ КТ В ПІДЗАТВОРНІЙ ОБЛАСТІ

В. В. Ільченко, Ш. Д. Лін, В. В. Марін, О. В. Третяк

Анотація. В даній статі досліджувалися структури польових транзисторів (ПТ) з шаром квантових точок (КТ), розташованим близько до каналу з високою електронною рухливістю на гетерограниці GaAs/AlGaAs. Було показано, що електричний заряд, що акумулюється в шарі КТ, може суттєво змінювати значення порогової напруги необхідної для відкривання каналу. Через кінетичну природу процесів захоплення та емісії в КТ диференціальна ємність, виміряна між витоком та затвором, має специфічний вигляд з кількома максимумами на C-V кривій в залежності від частоти тестового сигналу. Завдяки впливу накопичення заряду в КТ коефіцієнт передачі для транзистору з шаром КТ в підзатворній області демонструє ефект динамічної зміни провідності каналу.

Ключові слова: польові транзистори, квантові точки, GaAs/AlGaAs

ЭЛЕКТРОННЫЕ СВОЙСТВА ПТ СТРУКТУР СО СЛОЕМ КТ В ПОДЗАТВОРНОЙ ОБЛАСТИ

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Аннотация. В данной статье исследовались структуры полевых транзисторов (ПТ) со слоем квантовых точек (КТ), размещенным вблизи канала с высокой электронной подвижностью на гетерогранице GaAs/AlGaAs. Было показано, что электрический заряд, который аккумулируется в слое КТ, может существенно изменять значение порогового напряжения необходимого для открывания канала. Из-за кинетической природы процессов захвата и эмиссии в КТ дифференциальная емкость, измеренная между истоком и затвором, имеет специфический вид с несколькими максимумами на C-V кривой в зависимости от частоты тестового сигнала. Благодаря накоплению заряда в КТ коэффициент передачи транзистора со слоем КТ в подзатворной области демонстрирует эффект динамического изменения проводимости канала.

Ключевые слова: полевые транзисторы, квантовые точки, GaAs/AlGaAs

The FET structures with InAs QDs layer attract the considerable attention of the scientists and technologists because of existence of accumulation charge phenomenon in the QDs layer which are responsible for the dynamic memorizing in such kind of structures [1–6]. The main goal of this investigation was to design and study the structures with effective mechanisms of the accumulated in QDs charge influence on the conductivity of the 2-D gas channel placed nearby. In our case the inverted HEMT (high electron mobility transistor) structures were used because of number of unambiguous advantages for the charge capturing conditions to the QDs [7].

In this paper the investigation of the most important parameters of the FET structures with QDs layers under the gate area were performed, such as the threshold of the gate opening voltage and the frequency dependence of the transmission coefficient when QDs charge makes the influence on the conductivity channel. Because of high electron mobility of 2-D gas channel all filling and emission electron processes with QDs could be clear observed at these structures.

All structures were grown in National Nanodevice Laboratory of Chiao-Tung University (Hsinchu, Taiwan) by the MBE methods and using standard lithography technique. On Fig.1 the multi layer structure diagram with QDs placed under the Gate is shown.

Samples and their preparation

As it clearly follows from the Fig.1 Schottky barrier forms low conductivity layer over the channel (80 nm). At the applied Gate voltage QDs layer can be recharged and change the potential distribution under the gate area. Due to small distance between 2-D gas and QDs layer(20–30 nm) filling and emission electron processes with QDs layer can flow relatively fast then it was observed in the standard Schottky diode structures with QDs layer[4–6]. Al-GaAs basement (300 nm) of this structure provides good isolating confinement for the 2-D gas channel formed due to δ -doping of AlGaAs from the bottom side.



Fig. 1. The scheme of the experimentally grown structure.

Source and Drain contacts were formed by means of In electrodes and standard lithography technique with the different size masks of the gate length changed from 10 to 100 mkm.

As it is well-known there are several quantum levels in the 2-D gas channel can be placed on the boundary of the heterojunction GaAs/AlGaAs.

By voltage applied to the ohmic (Indium) contact the position of quasi Fermi level concerning to the quantum levels of QDs and 2-D gas channel can be changed easily. On Fig. 2 the energy diagram of the experimentally performed structure with negative and positive voltage applied to 2-D gas channel is shown.

Experimental results and their discussions

Using the energy diagram (see Fig. 2) it is possible to explain qualitatively two different states of FET structure which happen when QDs layer becomes empty or filled by electrons dependening on the voltage applied between Gate and Source U_{GS} .



Fig. 2. The energy diagram of the FET structure for the forward and reverse applied voltage between Gate and Source.

At first the transient characteristics of the investigated structures on the direct current were measured for negative and positive potential applied to the Gate. It should be mentioned that all structures could be switched off by negative U_{GS} .

On the one hand we want to get reliable evidence that FET structures are working properly. On the other hand we want to be sure that structures are good enough sensitive to the voltage applied to the Gate. To find differences in their characteristics the structures with QDs layer and without it were investigated for comparison. The families of transient characteristics obtained for the different external voltage applied between Source and Drain are presented on the Fig 3a and 3b.



Fig. 3. Transient characteristics of the FET structures with (a) and without (b) QDs layer under the Gate area taken at the different voltage between Source and Drain.

It is clear from the Fig.3a that current in the 2-D gas channel for the structures with QDs layer can be closed only at about -2 V applied to the Gate. At the same time the structure without QDs layer can be closed at positive applied potential +0.5 V.

This phenomenon looks quite understandable because QDs can accumulate large enough negative charge providing weak screening field effect in the space charge region under the Gate. So, to push out the carriers from the 2-D gas channel it is necessary to apply considerably large negative voltage to the Gate in this case than for the structures without QDs layer where electric field in the space charge region can push out the carriers from the 2-D gas channel when applied the Gate voltage is less then 0,5 V only. In other words, charge accumulated in QDs layer in the investigated structures can essentially shift the threshold voltage so, that to close this structure it is necessary to apply to the Gate more large negative potential to overhead the influence of QDs negative charge placed under the Gate.

As is follows from the Fig 3a the 2-D gas channel is already opened when applied to Gate voltage is equal to zero. Under this condition all QDs are filled by electrons. It is well known from the DLTS experiments performed in [7] for the similar experimental structures. It means that differences between transient characteristics obtained for the structures with QDs(Fig. 3a) and without QDs(Fig. 3b) at zero Gate should be definitely concern of the charge states of QDs layer. Thus, in order to close the 2-D gas channel it is necessary to make QDs empty. One of the possible ways to check this point is measure the frequency dependences of differential capacitance between Source and Gate.

The results of C-V measurements are good consistent with the results for transient characteristics obtained before (See Fig.4a and Fig.4b). There are two structures with QDs layer and without it measured for comparison as well.

As it is clearly observed C-V curves for the structures with QDs have the specific part with two peaks at small negative applied voltages between Gate and Source (U_{GS}). This part of C-V curves looks quite different from C-V curves for the structures without QDs layer obtained. It should be noted that differences of transient characteristics for these samples could be observed at same range of applied voltage U_{GS} when QDs could change their charge states. It is very representative that C-V curves demonstrate strongly marked frequency dependences for the structure with QDs layer at this range of applied voltage U_{GS} .

The explanation of the negative differential capacitance for the structures with QDs layers were clearly substantiated in [2–5]. There was shown that quantity of peaks and their dispositions are assigned of quasi Fermi level position concerning to quantum levels depending on applied voltage. When quasi Fermi level goes down at negative applied voltage U_{GS} the quantum level of QDs becomes empty. Otherwise when quasi Fermi moves up and crosses the quantum levels of 2-D gas channel they are progressively filled by electrons.

For positive applied voltage U_{GS} C-V curves have considerably negligible differences for the structures with and without QDs layer although C-V curves for these types of structures have also two large peaks but only at positive applied voltage U_{GS} . It can be explained because of much more important contribution in capacitance of charge accumulated on quantum levels in 2-D gas channel. Because of some differences in potential distribution there are some distinctive features for the samples with and without QDs should be mentioned but along with it two diffused and asymmetrical frequency dependent peaks could be good visible on C-V curves for both types of the investigated structures with and without QDs layer inside.



Fig. 4. C-V characteristics taken between Gate and Source for the differential capacitance measured on different frequencies for the structures with (a) and without (b) QDs layer under the Gate.

The same conclusion can be done on the ground of the analysis of frequency dependence of C-V characteristics. The magnitudes of frequencies when filling process of QDs can not follow for alternative testing signal reach the same values 10–20 kHz that in the paper where frequency dependences of negative differential capacitance for the Schottky diod with QDs built-in space charge region was studied in detail [3-5]. The fragments of C-V curves obtained taken at different frequency of alternative testing signal for the samples with QDs under the Gate area are shown on Fig. 5.



Fig. 5. Scaled-up fragments of C-V curves for the negative U_{GS} taken at different frequency of testing signals for the FET structures with QDs layer.

It is followed from Fig.5 that partition of C-V curves taken at negative voltage U_{GS} have two points of kinking suppose to be connected with two quantum levels (lowest and second one) of QDs[7–8]. At more then -1,5–1,75 V applied voltage U_{GS} all quantum levels in QDs are totally discharged then capacitance essentially decreased almost to zero because charge inside the structure are missed. It should be noted that this value of applied voltage U_{GS} is exactly equal to the threshold voltage when 2-D gas channel becomes off (See Fig.3).

The investigation of the transmission coefficient on the alternative current were performed to determine the limiting rate of recharging processes in QDs. It should be mentioned that modulation of the conductivity of 2-D gas channel in our case can be able on the frequency when charge in QDs can follow for the changing of testing signal applied to the Gate.

To perform such kind of investigation the separate experimental setup was used. The main parts of this setup were the generator of periodic signals with different frequency and selective amplifier. Both of these devices could be smoothly adjust in wide enough range of frequency. The testing signal could be applied to the structure in the background of definite offset voltage applied between Gate and Source which was determined the position of quasi Fermi level concerning to the quantum level of QDs. The block-scheme of this setup is presented on the Fig.7.



Fig. 6. Block-scheme of the setup for the frequency dependences of transmission coefficient investigation.

The selective amplifier could be switched to calibrated mode with definite coefficient of amplification. Then the signal from output of the selective amplifier was treated by analog-digital converter of the computer.

All measurements are carried out with amplitude 50 mV of testing signal for several frequencies from 1 kHz to 150 kHz and presented on Fig.7.



Fig. 7. The dependence of transmission coefficient from the offset voltage applied to the Gate U_{GS} taken at different frequency of testing signal.

Fig.7 explicitly demonstrates that transmission coefficient becomes equal zero when offset voltage U_{GS} applied to the Gate achieves -2.0 V when (as it was clear shown from experiments with threshold voltage for U_{GS}) 2-D gas channel becomes switched

off. In the meantime at the offset voltage U_{GS} about -1 V the max of transmission coefficient was clearly revealed. This value of the offset voltage corresponding to the position of the second peak in C-V curves when the recharging process of lowest level in QDs supposed to be occurred. As it is clear from Fig.7 the transmission coefficient measured under these conditions was essentially frequency dependent as well. But this time the recharging process in QDs and connected with it modulation of 2-D gas channel conductivity demonstrates more weak frequency dependence then in C-V measurements. To explain that the participants of higher QDs levels with considerably short time of recharging process can be naturally assumed. Very fortunately at room temperature we can observe only some average results corresponding to the wide enough distribution function. In the meantime the max of transmission coefficient can be relatively clear visible at definite value of applied voltage U_{cs} .

Conclusion

Electrical charge accumulated in InAs QDs layer placed close to the 2-D gas channel with high electron mobility on the boundary of heterojunction GaAs/AlGaAs in FET structures causes the essential modulation of their conductivity. The existence of QDs layer in FET structures is notably shift in negative value (-2 V) the threshold voltage applied to the Gate to open the channel. The QDs layer under the Gate area of the FET structures can essentially influence on the differential capacitance measured between Gate and Source. There are several peaks of differential capacitance caused by QDs layer existence clearly observed at room temperature. The limitation of the recharging rate of the QDs is the main reason of frequency dependences of differential capacitance at small negative (less then -2 V) when modulation of channel conductivity caused by charge accumulation in QDs layer. The transmission coefficient in this case for the FET structures demonstrated the specific maximum at -1 V depending from voltage applied to the Gate.

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References

- Balocco C., Song A. M., Missous M.. Room-temperature operations of memory devices based on selfassembled InAs quantum dot structures//Appl. Phys. Lett. – 2004. Vol. 88, P. 5911–5913.
- Chiquito A. J., Pusep Yu.A. et al. Capacitance spectroscopy of InAs self-assembled quantum dots embedded in a GaAs/AlAs superlattice // J. Appl. Phys. 2000. Vol.88, No.4. P. 1987–1991.
- Chiquito A. J., Pusep Yu. A., Mergulhao S., and Galzerani J. C. Capacitance-voltage profile in a structure with negative differential capacitance caused by the presence of InAs/GaAs self-assembled quantum dots //Phys.Rev. 2000. Vol. 61, P. 5499 5504.
- Lin S. D., Ilchenko V. V., Marin V. V.et al. Observation of the negative differential capacitance in Schottky diodes with InAs quantum dots near room temperature// Appl. Phys. Lett. 2007. Vol.90, P. 263114(1–3).
- Ilchenko V. V., Lin S. D., Marin V. V., Shkil N. V., Panarin K. Y., Buyanin A. A., Tretyak O. V. Room temperature negative differential capacitance in selfassembled quantum dots. — Journal of Physics D: Appl. Phys. 2008. — Vol. 41, p.p. 235107(1–4).
- Chen J. F., Chen C. C., Chiang C. H., Chen Y. F., Wu Y. H. and Chang L. Bimodel onset strain relaxation in InAs quantum dots with an InGaAs capping layer. — Applied Phys. Lett. 2010. — Vol. 97, p.p. 092110(1–3).
- Ilchenko V. V., Lin S. D., Lee C. P., Tretyak O. V. Deep level transient spectroscopy characterization of InAs self-assembled quantum dots. // Journ. Appl. Phys., 89, No.2, 2001, 1172–1174.
- Ilchenko V. V., Lin S. D., Marin V. V., Tretyak O. V. Electrical properties of FET structures with QDs layer. Proceedeing of IV Ukrainian scientific conference on physics of semiconductors (Zaporizhya, 15–19 of September 2009p). V.1. p.p.108–109.