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MODELING OF ANALOG-TO-DIGITAL SIGNAL CONVERTERS FOR SENSOR MICROSYSTEMS IN THE MICROWIND SOFTWARE

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Abstract. For the results of simulating the operation of analog-digital converters, we chose such a converter as the serial approximation ADC (SAR ADC). A sequential approximation ADC is a type of analog-to-digital converter that converts a continuous analog waveform to a discrete digital representation by binary search through all possible quantization levels before finally converging on a digital output for each conversion. There are three important blocks in the SAR ADC architecture: the sample and hold circuit (Sample and Hold, S/H), the comparator, and the SAR block. The topology and principle of operation of which was modeled in the Micro Wind software environment.

Keywords: analogue-to-digital converter, MicroWind software, submicron technology

МОДЕЛЮВАННЯ АНАЛОГО-ЦИФРОВИХ ПЕРЕТВОРЮВАЧІВ СИГНАЛІВ ДЛЯ СЕНСОРНИХ МІКРОСИСТЕМ У ПРОГРАМНОМУ СЕРЕДОВИЩІ MICROWIND

Л. І. Никируй, Р. В. Ільницький, М. Ф. Павлюк

Анотація. Для моделювання роботи аналого-цифрових перетворювачів обрано перетворювач АЦП послідовного наближення (SAR ADC). АЦП із послідовним наближенням – це тип аналого-цифрового перетворювача, який перетворює неперервну аналогову форму сигналу

в дискретне цифрове представлення за допомогою двійкового пошуку через усі можливі рівні квантування перед остаточним зближенням до цифрового виходу для кожного перетворення. В архітектурі SAR ADC є три важливі блоки: схема вибірки та зберігання (Sample and Hold, S/H), компаратор і блок SAR. Топологія та принцип роботи змодельовано в програмному середовищі Micro Wind.

Ключові слова: аналого-цифровий перетворювач, програмне забезпечення MicroWind, субмікронна технологія

Introduction

The main application of the sample-and-store scheme is in ADC. This function block processes the analog input signal and stores the value between tact. Many ADC topologies require a stable input signal, which is provided by the S/H circuit [1]. This reduces ADC error caused by internal delay variations. Sometimes this circuit element is called Track and Hold (T/H). Typically, a sample-and-hold circuit contains a switch and a capacitor. In trace mode, when the sampling signal is high and the switch is connected, it traces the analog input signal. It then holds the value when the sample signal goes low in the hold mode. Figure 1 shows a model of the S/H scheme in DSCH 3.5

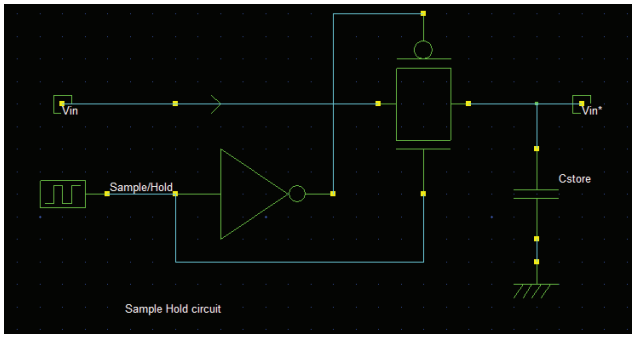

Fig. 1. Model of the sampling and storage functional block in DSCH 3.5.

Results and discussion

During binary search, the analog input signal is sampled and its sampled value is saved by the S/H circuit. Two signals are applied to the input: one is an analog input signal applied to the transfer switch, and the other is a square-wave sampling signal applied to the CMOS rather than the gate, which is implemented using advanced MOSFETs to sample the analog input. The implementation of the sampling and storage block topology was carried out in the MicroWind software environment (Fig. 2). [2,3].

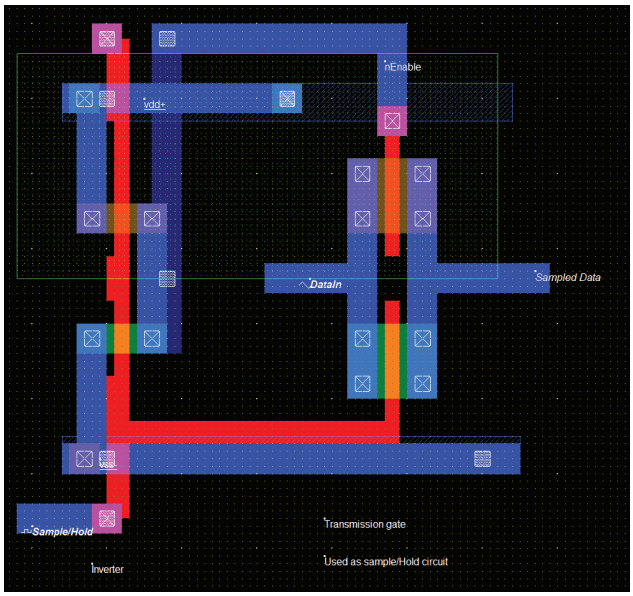

Fig. 2. Topology of the sample and storage unit.

The input is a continuous analog signal, we sample it and obtain a specific digitized value that is stored at the output of the S/H circuit until the input is sampled again, i.e. the sampling signal goes low. In the above circuit, there are two types of signals, one is the input analog voltage and the other is the sample voltage. So, depending on the sampling voltage, a signal is generated. In the case of high sample voltage, the analog voltage is held at a certain level for a certain time depending on the on-time of the square-wave sample signal [4–6]. S/H is usually implemented using a capacitive matrix, and the difference between successive samples is taken. The input signal is sampled on the top plates when using load switches. This increases installation speed and input bandwidth. And at the same time the lower plates are reset to V_{ref}.

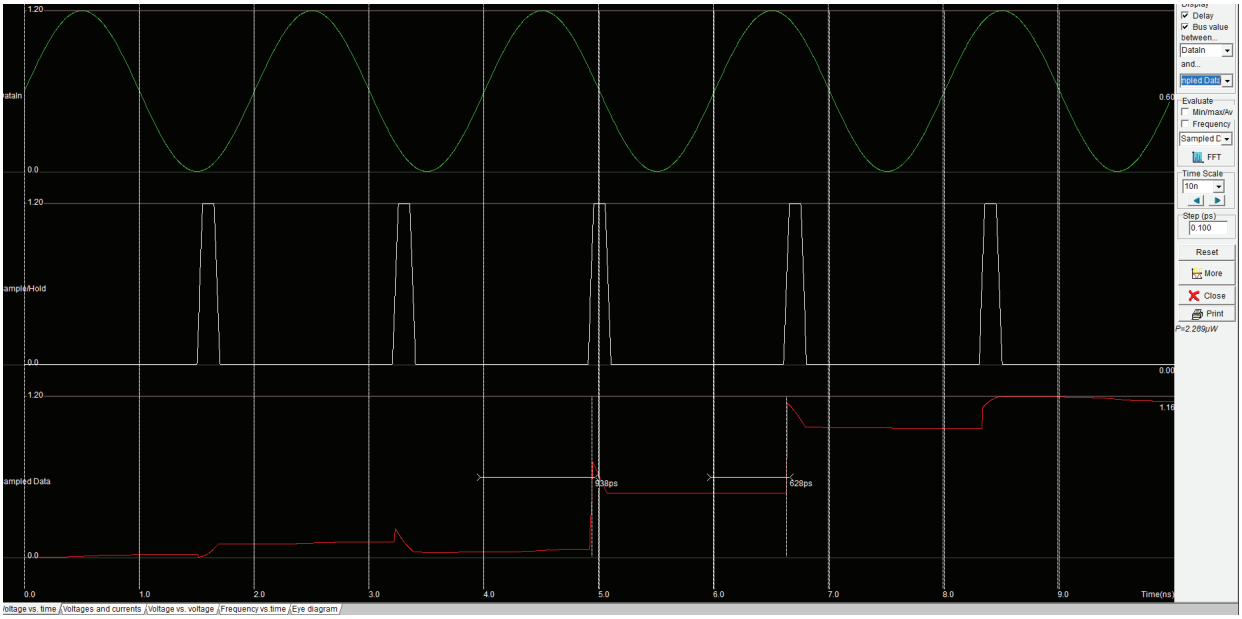

Fig. 3. S/H block simulation result.

The comparator is the only analog unit of the SAR ADC and performs the actual conversion. It compares the analog input signal to the analog output of the DAC and generates a digital output of «0» or «1» to be used in the SAR logic. The comparator consists of two input terminals, +V_in and -V_in, where the analog input voltage is supplied.[7–8]. If the voltage at +V_in is less than -V_in, then at the output of the comparator V_out, «0» is output. But if -V_in is greater than +V_in, then «1» is output. Therefore, comparators are sometimes referred to as «single-bit ADCs». The common mode range of a conventional comparator is limited by current-voltage (I–V) operations.

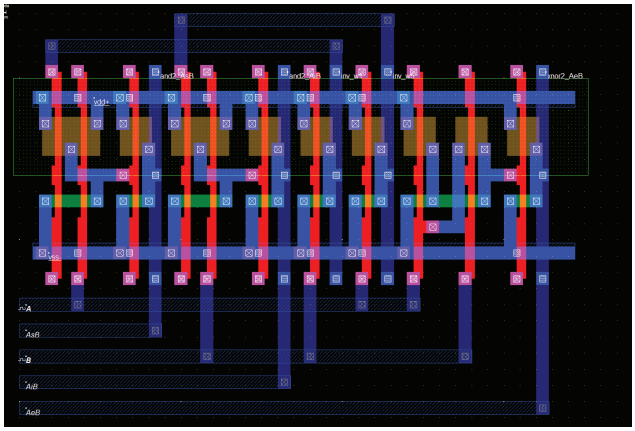

Fig.4. A comparator topology built in MicroWind is demonstrated.

And while in the middle of the power range, switching may not be possible. Therefore, a latched comparator can be used for a wide range of input signal oscillation. The offset error in this case depends on the MOSFET and the resistors. This offset does not affect the overall linearity, but does affect the global offset, which can be removed digitally. Traditionally, the reset phase stops the comparator after the proper input voltage has been established.

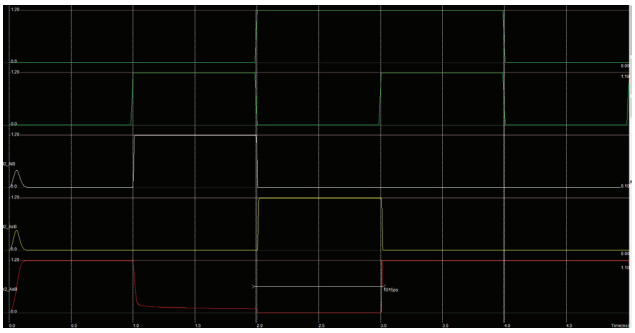

Fig.5. The result of simulating the operation of the comparator in MicroWind.

The last block of the SAR ADC is the sequential approximation control register itself. Serial approximation register (SAR) control logic defines each bit sequentially. The SAR register contains N-bits for an N-bit ADC. There are 3 possible states for each bit, it can be set to «1», reset to «0» or keep its value. In the first step,

the MSB is set to «1» and the other bits are reset to «0», the digital code is converted to an analog value via a DAC. The analog signal at the output of the DAC is applied to the input of the comparator and compared with the sampled input. Based on the result of the comparator, the SAR controller determines the value of the MSB. If the input signal is higher than the DAC output, the MSB remains at «1», otherwise it is reset to «0». The remaining bits are defined in the same way. In the last cycle, the converted digital code is stored. Thus, an N-bit SAR ADC requires N+1

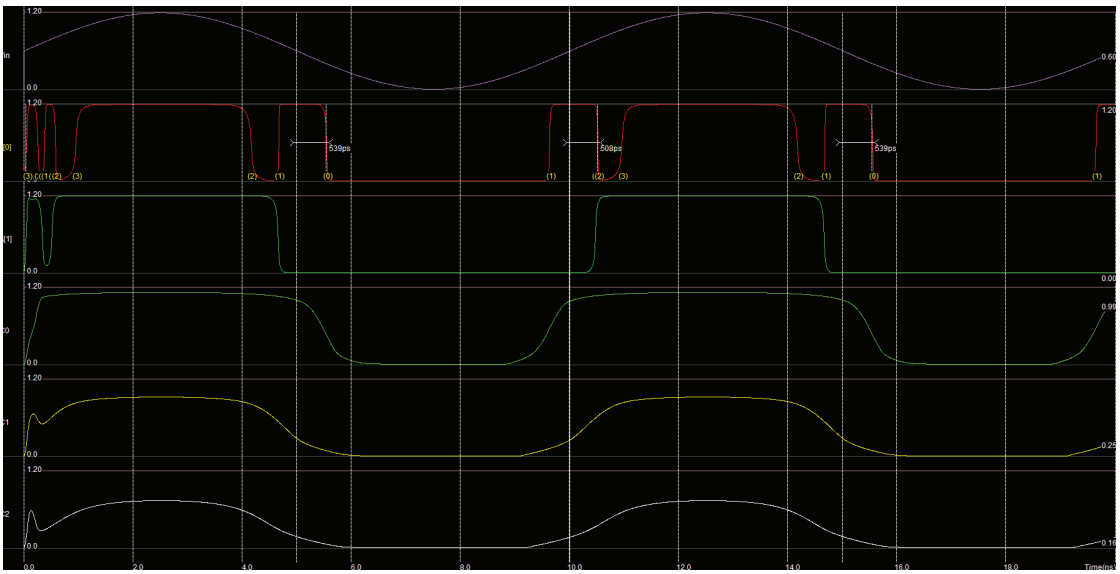

Fig. 6. SAR-ADC simulation result.

clock cycles to perform the conversion. SAR is a combination of counter and combinational logic. This helps achieve higher ADC resolution, but also changes power consumption and signal propagation delay accordingly [9].

A possible implementation of the topology of such a signal converter is presented in Fig. 7. It uses the previously mentioned function blocks: S/H. DAC, Comparator and SA Register.

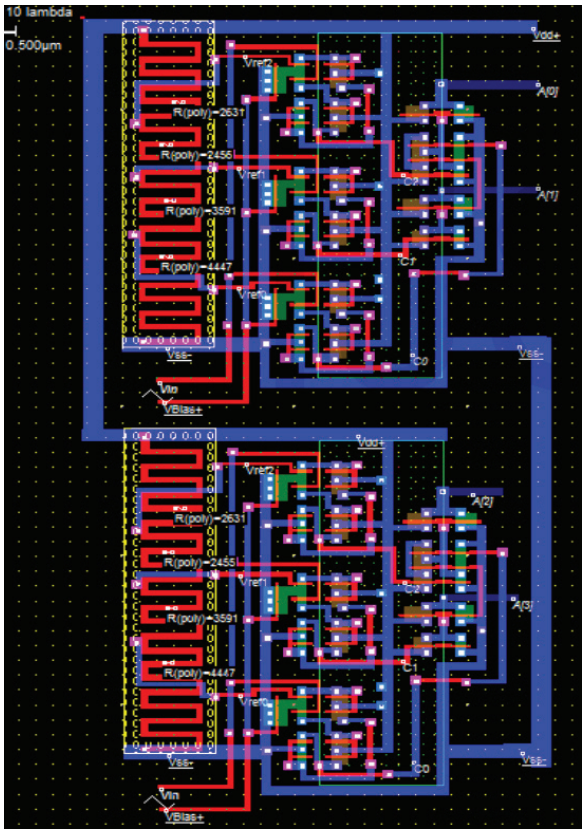

Fig. 7. Modeled SAR ADC topology in the micro wind software environment.

Conclusion

For low-rate samples, we can sample from the lower bits. This therefore results in low power consumption without affecting linearity. The comparator bias voltage can also be formed as a voltage source with the output of the S/H circuit, which involves adding a bias to the analog input. But the main disadvantage of this technology is the high power consumption due to the isolated S/H circuit. These types of circuits are called internal S/H circuits and are typically implemented using a binary weighted capacitance. Thus, the MicroWind 3.1 software application

was used to model and design the operation of the DAC, as it is an open-source software tool for all users that allows the design and simulation of an integrated circuit at the physical description (IC) level. Also, the DSCH3.5 program is a logic editor and simulator of electronic circuits. DSCH3.5 is used to verify the architecture of the logic circuit before starting the microelectronics design.

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Summary

The purpose of the submission is a computer simulation of analog-digital converters, we chose such a converter as the serial approximation ADC (SAR ADC).

It is shown for low-rate samples, we can sample from the lower bits. This therefore results in low power consumption without affecting linearity. The comparator bias voltage can also be formed as a voltage source with the output of the S/H circuit, which involves adding a bias to the analog input. But the main disadvantage of this technology is the high power consumption due to the isolated S/H circuit. These types of circuits are called internal S/H circuits and are typically implemented using a binary weighted capacitance. Thus, the MicroWind 3.1 software application was used to model and design the operation of the DAC, as it is an open-source software tool for all users that allows the design and simulation of an integrated circuit at the physical description (IC) level. Also, the DSCH3.5 program is a logic editor and simulator of electronic circuits. DSCH3.5 is used to verify the architecture of the logic circuit before starting the microelectronics design

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Реферат

Метою дослідження є комп’ютерне моделювання дизайну аналого-цифрових перетворювачів обрано перетворювач АЦП послідовного наближення (SAR ADC).

При виконанні дослідження здійснено аналіз архітектури існуючих типів цифро-аналогових перетворювачів, застосовано комп’ютерні симуляції у середовищі MicroWind.

Показано, що для низькошвидкісних вибірок можна робити вибірку з нижчих бітів. Таким чином, це призводить до низького енергоспоживання без впливу на лінійність. Напруга зміщення компаратора також може бути сформована як джерело напруги з виходом схеми S/H, що передбачає додавання зміщення до аналогового входу. Але основним недоліком цієї технології є високе енергоспоживання через ізольовану схему S/H. Ці типи електричних кіл називаються внутрішніми кола S/H, і, зазвичай реалізуються з використанням двійкової зваженої ємності. Таким чином, програмний додаток MicroWind 3.1 використовувався для моделювання та проектування роботи ЦАП, оскільки це програмний інструмент із відкритим вихідним кодом для всіх користувачів, який дозволяє проектувати та моделювати інтегральну схему на рівні фізичного опису (IC). Логічним редактором і симулятором електронних схем є програма DSCH3.5, яка використовується для перевірки архітектури логічної схеми перед початком проектування мікроелектроніки.

Ключові слова: цифро-аналоговий перетворювач, програмне забезпечення MicroWind, субмікронна технологія